UNCLASSIFIED

AD 402 887

Reproduced
by the

DEFENSE DOCUMENTATION CENTER

FOR

SCIENTIFIC AND TECHNICAL INFORMATION

CAMERON STATION, ALEXANDRIA, VIRGINIA

UNCLASSIFIED

NOTICE: When government or other drawings, specifications or other data are used for any purpose other than in connection with a definitely related government procurement operation, the U. S. Government thereby incurs no responsibility, nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use or sell any patented invention that may in any way be related thereto.

AFCRL-63-67

402 887

RADIO CORPORATION OF AMERICA
RCA LABORATORIES

EVAPORATED THIN-FILM DEVICES

BY

P. K. WEIMER
H. BORKAN
F. V. SHALLCROSS

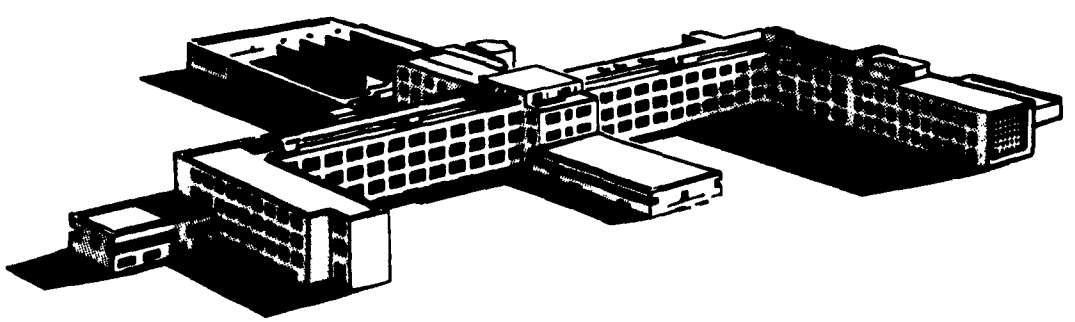
CONTRACT NO. AF19(628)-1617
PROJECT NO. 4608, TASK NO. 460804

SCIENTIFIC REPORT NO. 2

MARCH 10, 1963

PREPARED FOR

ELECTRONIC RESEARCH DIRECTORATE
AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
OFFICE OF AEROSPACE RESEARCH
UNITED STATES AIR FORCE
BEDFORD, MASSACHUSETTS



DAVID SARNOFF RESEARCH CENTER
PRINCETON, NEW JERSEY

Requests for additional copies by Agencies of the Department of Defense, their contractors, and other Government agencies should be directed to the:

ARMED SERVICES TECHNICAL INFORMATION AGENCY
ARLINGTON HALL STATION
ARLINGTON 12, VIRGINIA

Department of Defense contractors must be established for ASTIA services or have their "need-to-know" certified by the cognizant military agency of their project or contract.

AFCRL-63-67

EVAPORATED THIN-FILM DEVICES

PREPARED BY
P. K. WEIMER
H. BORKAN
F. V. SHALLCROSS

RADIO CORPORATION OF AMERICA
RCA LABORATORIES
PRINCETON, NEW JERSEY

SCIENTIFIC REPORT NO. 2

FOR THE PERIOD
DECEMBER 1, 1962 TO FEBRUARY 28, 1963

CONTRACT NO. AF19(628)-1617
PROJECT NO. 4608
TASK NO. 460804

MARCH 10, 1963

PREPARED FOR

ELECTRONIC RESEARCH DIRECTORATE
AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
OFFICE OF AEROSPACE RESEARCH
UNITED STATES AIR FORCE
BEDFORD, MASSACHUSETTS

ABSTRACT

An improved electrode arrangement for the insulated-gate thin-film transistor has yielded higher performance and greater ease of fabrication. "On-to-off" current ratios of 10^7, input resistance exceeding 10^{10} ohms, and gain-bandwidth products of 25 megacycles have been obtained with polycrystalline cadmium sulfide films. By depositing all electrodes on top of the semiconductor, maximum freedom in processing the semiconductor layer is obtained. A novel type of field-effect diode is described.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

I. INTRODUCTION

Recent advances in the physical understanding and in the technology of the insulated-gate thin-film transistor has led to TFT's of higher performance and simpler construction. Section II describes the design and operational characteristics of the improved form of TFT in which all electrodes are deposited over the top of the semiconductor layer. The results have been extended to the construction of CdSe TFT's and to other integrated-circuit components including resistors and a novel form of field-effect diode. In Section III further results of mobility measurements and thin-film materials studies are reported.

II. THE COPLANAR-ELECTRODE TFT

During the past year a new form of insulated-gate thin-film transistor possessing significant advantages over the earlier form of TFT has been developed. Greater ease of fabrication and improved performance has been obtained without sacrificing the wide versatility for integrated-circuit applications inherent in thin-film transistors deposited upon an insulating substrate. Although the coplanar-electrode structure was described in a paper on the TFT,[1] the techniques for fabricating superior units of this type have been developed more recently. Some preliminary results of this work were reported in the Scientific Report No. 1 of this contract,[2] but the present discussion describes in greater detail the fabrication, physical processes, and performance of the new units. Because of the greater ease of fabrication, it has been convenient to use the coplanar units for various types of field-effect studies not specifically requiring the coplanar structure. The coplanar techniques have also been applied successfully to semiconductors other than cadmium sulfide. These include CdSe and ZnO.

A. CONSTRUCTION OF THE COPLANAR TFT

Figure 1 compares the geometrical configuration of two coplanar TFT's with the earlier "standard" staggered structure. The order of deposition of the layers is shown in Table I. A technological advantage in the use of the coplanar structure lies in the fact that the semiconductor

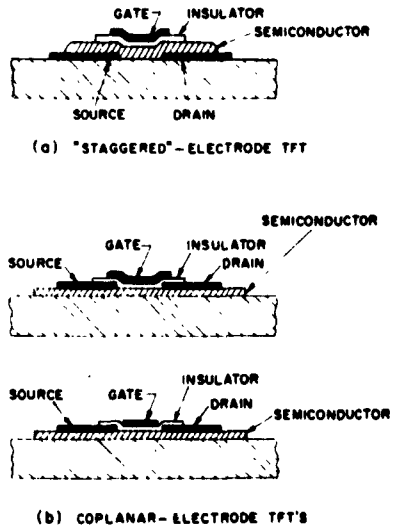


Fig. 1. Cross-sectional drawings of two coplanar-electrode TFT's compared with the earlier "staggered" structure.

TABLE I

FABRICATION PROCEDURE FOR MAKING THIN-FILM TRANSISTORS

STAGGERED TFT STRUCTURE			
STEP	SEMICONDUCTOR EVAPORATOR	EXTERNAL PROCESSING	PRECISION-MASK EVAPORATOR
I	Semiconductor deposition	Semiconductor bake	S-D evaporation
II			
III			
IV			Insulator deposition
V			Gate deposition
COPLANAR TFT STRUCTURE			
STEP	SEMICONDUCTOR EVAPORATOR	EXTERNAL PROCESSING	PRECISION-MASK EVAPORATOR
I	Semiconductor deposition	Semiconductor bake	
II			
III			S-D deposition
IV			Insulator deposition
V			Gate deposition

deposition and processing can be done prior to the laying down of the electrodes, thus permitting processing procedures not compatible with the underlying electrodes. Greater accuracy can also be obtained in the positioning of the source, gate, and drain electrodes since the semiconductor deposition step does not need to be interposed. As noted in Table I the high substrate temperature required for the semiconductor evaporation made it necessary with the staggered structure to remove the sample from the precision evaporator for steps II and III and then to re-align the sample in the precision evaporator for steps IV and V. With the coplanar structure, source, drain, insulator, and gate are evaporated in sequence in one setup in the precision evaporator. No precise pre-registery step is required since the location of the semiconductor area relative to the final structure is less critical. Source and drain can either be done in sequence or simultaneously, depending upon the type of mask and whether symmetrical or rectifying characteristics are desired.

The order in which the source-drain electrodes and the insulator are deposited in the coplanar structure plays an important role in the final operation of the device. The arrangement shown in which

insulator overlaps the source and drain is advantageous from the standpoint of reducing surface leakage paths and in permitting the gate to be very close to the source and drain. The overlapping insulator permits the gate actually to overlap the source and drain without danger of a direct short. However, in deciding the order of depositing the source-drain or insulator, one has to consider the scatter of evaporating material which can deposit under the mechanical masks. If the insulator were evaporated first, the danger of metal scattering into the critical gate interface region is avoided, but the opportunity would then exist for insulator material to be scattered into the source contact area. Since optimum performance of the field-effect transistor requires a low-impedance contact at the source electrode for injection of majority carriers, it was found preferable to evaporate the source electrode first to ensure an ohmic contact.

The choice of a source-electrode material is doubly critical since it must make a low-impedance contact to the semiconductor, and the material scattered into the gap area must not introduce objectionable surface states. Since evaporated gold underlying the CdS layer made a reasonably low-impedance contact in the staggered structure, gold was tried first for the overlying source electrode in the planar structure. Gold electrodes were found to fall short on both accounts listed above. The contact obtained was blocking instead of ohmic (in good agreement with others who have evaporated gold contacts onto CdS single crystals), and the scattered gold introduced undesirable acceptor-like surface states into the gap region. The latter statement was verified in separate experiments on the effect of thin gold layers on the CdS-insulator interface region of the staggered TFT having underlying electrodes.

Aluminum was found to make a satisfactory contact to CdS (and to CdSe), if evaporated under carefully controlled conditions. If evaporated too slowly, however, a high-impedance contact is obtained which gives rise to a particular type of operating characteristic (called "crowding") discussed in Section II.D.2. Some excellent units have also been made having aluminum electrodes with a thin interface of indium between the aluminum and the semiconductor.

The requirements for the insulator and gate of the coplanar TFT are the same as in the staggered structure. Silicon monoxide and calcium fluoride have been used most frequently for the insulator, but other materials are being investigated. The gate electrode is usually either aluminum or gold.

B. DESCRIPTION OF THE OPERATING CHARACTERISTICS OF THE COPLANAR TFT

The overall operating characteristics of the coplanar insulated-gate transistor are approximately the same as those obtained with the staggered structure.[2] (See Fig. 2.) Well-saturated

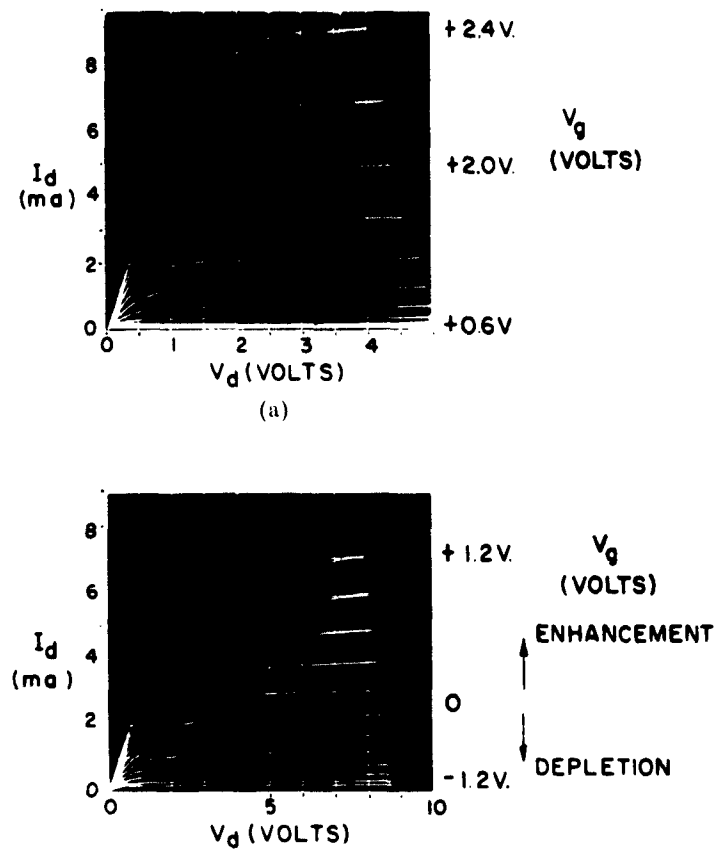


Fig. 2. Current-voltage characteristics for (a) an enhancement-type CdS coplanar TFT, and (b) a depletion-type CdS coplanar TFT.

current-voltage characteristics of either the enhancement or depletion type agree very closely with curves predicted theoretically from the field-effect analysis.[2,3,4] In the earlier work (summarized in Fig. 3) it was shown that the drain current I_d up to the knee of the curve is given by

$$I_d = \frac{\mu C_g}{L^2}\left[(V_g - V_o)V_d - \frac{V_d^2}{2}\right], \tag{1}$$

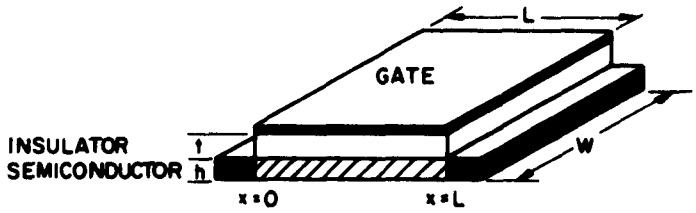
where μ = drift mobility in the semiconductor (assumed to be constant),
C_g = total gate capacitance,
L = length of gap between source and drain electrodes,

V_g = applied gate voltage relative to the source potential,

V_d = applied drain voltage, measured relative to source potential,

and V_o = gate voltage required for the onset of drain current.

For finite I_d, $(V_g - V_o)$ must be positive. V_o is negative for a depletion-type unit having an initial conductivity at zero gate bias, and zero or positive for an enhancement-type unit. By differentiating Eq. (1) it may be shown that the knee of the saturated I_d vs. V_d characteristic occurs at a drain voltage equal to $V_g - V_o$.



LET Δn = CARRIER DENSITY INDUCED BY FIELD EFFECT:

$$\Delta n \text{ (ELECTRONS/cm}^2) = \frac{C_g[V_g - V(x)]}{q \cdot LW}$$

LET n_o = CHANGE IN CARRIER DENSITY PRODUCED BY SURFACE STATES INITIALLY PRESENT

$$I_d = W \cdot \bar{n}_s \cdot q\,\mu\, E_x = Wq\mu\,(n_o + \Delta n)\,\frac{dV(x)}{dx}$$

$$I_d = Wq\mu \left\{ n_o + \frac{C_g[V_g - V(x)]}{q \cdot LW} \right\} \frac{dV(x)}{dx}$$

AFTER INTEGRATION:

$$I_d = \frac{\mu C_g}{L^2} \left\{ \left(\frac{n_o\, qLW}{C_g} + V_g \right) V_d - \frac{V_d^2}{2} \right\}$$

DEFINITION OF V_o, THE BUILT-IN GATE BIAS:

$$\frac{n_o\, qLW}{C_g} \equiv -V_o$$

WHENCE:

$$I_d = \frac{\mu C_g}{L^2} \left\{ (V_g - V_o) V_d - \frac{V_d^2}{2} \right\}$$

$$\frac{g_m}{C_g} = \frac{\mu V_d}{L^2}$$

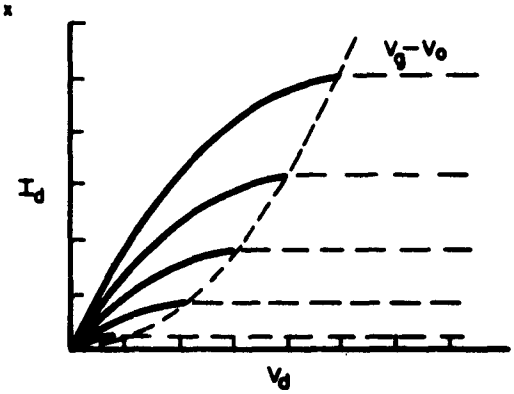


Fig. 3. Derivation of the current-voltage characteristic of the insulated-gate transistor (valid up to the "knee" of the curve).

The fabrication of the coplanar units has been far more satisfactory than the staggered units in that failures to obtain high-voltage amplification factors are relatively rare. The ratio of maximum I_d to pinched-off I_d has exceeded 10^7. Maximum transconductances of 10,000 to 20,000 μmhos have

been obtained with polycrystalline cadmium sulfide for an input capacitance of 25 pf at zero gate bias. D.C. gate resistance has been measured to be greater than 10^{10} ohms. Measurements demonstrating improved gain-bandwidth products are described in Section II-C.

C. ELECTRICAL MEASUREMENTS ON COPLANAR CdS TFT's

The electrical characteristics of planar-type, thin-film transistors are quite similar to those of the staggered structure. Typical drain, capacitance, temperature, and switching-speed measurements of the staggered-structure TFT's were reported in Scientific Report No. 1.[2] The drain characteristics of the two types of units are similar and the following statements are true for both types: (1) At low drain voltage, below the onset of current saturation, the output conductance is linear with gate voltage. (2) The drain voltage at the knee is proportional to the gate voltage-plus-a-constant. (3) In the current saturation region above the knee, the transconductance is proportional to the square root of the drain current. The measured transconductances of both types of units have been comparable.

Capacitance data were taken on several planar-type TFT's. A typical capacitance characteristic, measured at 100 kc, is shown in Fig. 4. The unit exhibits an increase in total gate capacitance, C_g, with zero drain volts applied, from about 10 to 50 pf as the gate voltage is

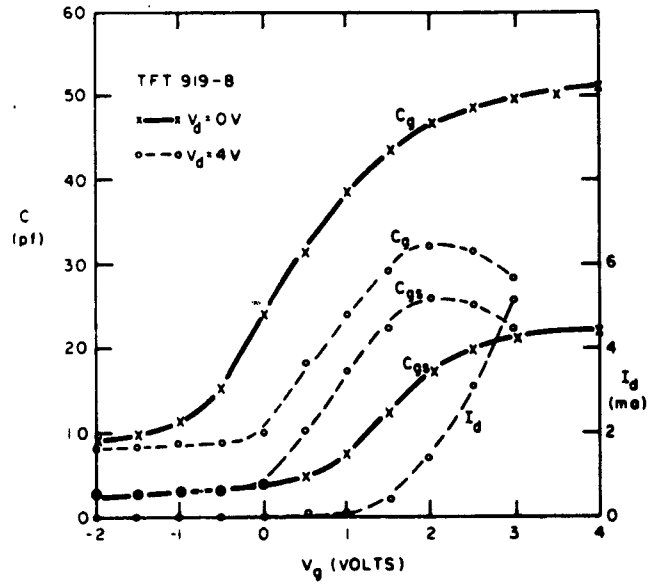


Fig. 4. Capacitance and transfer function of an enhancement-type, coplanar-electrode cadmium sulfide TFT.

increased from −2 to +4 volts. The comparable change observed in a staggered-electrode TFT is much less. With zero drain volts applied, this total gate capacitance divides according to the geometrical position of the gate relative to the other two electrodes. In the unit measured the capacitance between gate and source, C_{gs}, is somewhat less than between gate and drain, $C_{gd} = C_g - C_{gs}$. Inspection of this particular TFT under the microscope confirmed that the gate is closer to the drain than to the source.

The dashed curves were taken with 4 volts applied to the drain. The planar units do differ somewhat from the staggered units in the capacitances measured in the saturation region. The staggered structure exhibits a C_{gs} vs. V_g maximum at the onset of drain current. Planar units usually exhibit a maximum at high drain current. Invariably, in staggered TFT's the maximum capacitance at high drain voltage is almost as large as the asymptotic value obtained with zero drain volts. In the planar structure the maximum is somewhat smaller. However, both types of units have the major portion of C_g (measured at high drain voltage) appearing between gate and source electrodes and the minor portion between gate and drain. Since both the drain characteristic and the capacitance characteristic of the planar structure are similar to that observed in the staggered structures, the basic field-effect mechanism analyzed and described in the earlier report applies equally well to the planar geometry. There seems to be no major difference in operating mechanism between the two different structures.

The transfer characteristic, I_d vs. V_g, of the unit whose capacitances are described, is also shown in Fig. 4. Note that this TFT is an enhancement type with the onset of drain current occurring for V_g = 1 volt. The transconductance is about 4500 μmhos (determined from the slope of the transfer characteristic) and C_g is about 30 pf; both were measured with 3 volts applied to the gate. These yield a gain-bandwidth product of about 25 mc.

A planar TFT, similar to the one described above, was operated as both a low-pass and bandpass amplifier. The gain vs. frequency characteristics are shown in Fig. 5. The quiescent

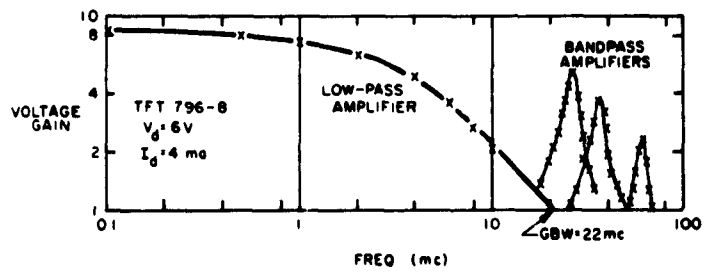


Fig. 5. Low-pass and bandpass amplifier characteristics of a single-stage cadmium sulfide coplanar TFT.

operating conditions used in these tests yielded an operating transconductance of about 5000 μmhos, while the measured C_g was approximately 30 pf. As a low-pass amplifier, it produced a voltage gain of about 8.5 from D.C. up to 2.6 mc (down 3 db) using a load resistor of 3000 ohms. This is an operating gain-bandwidth product of about 22 mc. The test was made with a low-impedance signal source but additional output capacitance, simulating a second TFT stage, was included.

Three different bandpass amplifier characteristics using this unit are also shown in Fig. 5. An inductance in parallel with the inherent circuit capacitance serves as the load impedance in all cases. The three amplifiers were resonant at 25 mc, 36 mc and 60 mc. Note that a voltage gain of 2.5 was obtained at 60 mc. The measured gain-bandwidth product at a center frequency of 60 mc was about 17 mc, down somewhat from the low-pass amplifier data. This may indicate that some degradation in effective transconductance is occurring at this frequency.

Switching-speed data taken on this unit show drain-current transitions from off to on and from on to off in about 30 nsec. The waveforms are similar to Fig. 17 in Scientific Report No. 1.[2]

The dependence of drain current in the planar thin-film transistor with temperature is less severe than in the staggered structure. Typical variation of drain current for a planar-type TFT under fixed gate and drain voltages is shown in Fig. 6. The drain current is plotted as a function

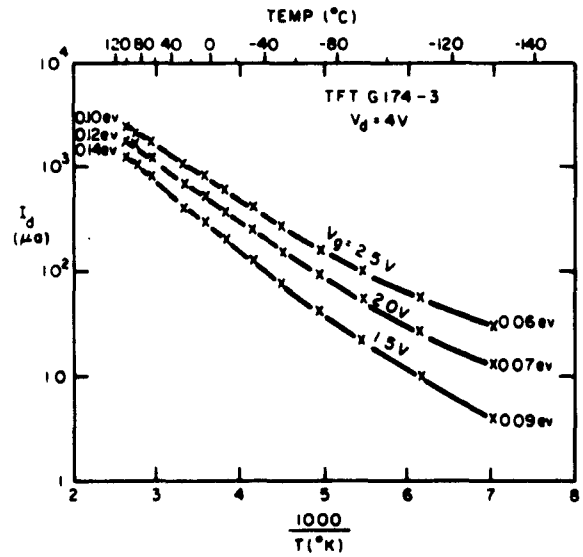


Fig. 6. Drain current plotted against the reciprocal temperature for a coplanar CdS TFT with constant electrode voltages applied.

of the reciprocal of the absolute temperature. The slopes of the curves in this graph are related to activation energy levels which are listed at the ends of the curves. Note that the computed activation energy levels for the staggered structure (given in Fig. 18, Scientific Report No. 1[2]) are about 50% greater than for the planar structure. Less dependence on temperature in the planar units may be due to the presence of barriers in the bulk of the cadmium sulfide. Conduction through the bulk of the semiconductor occurs in the staggered design but does not occur in the planar construction.

D. PHYSICAL ASPECTS OF TFT DESIGN

1. Control of the Built-in Gate Bias V_o

For optimum performance of integrated circuits incorporating insulated-gate TFT's, it is necessary to have sufficient control of the fabrication procedure to yield TFT's whose gate bias for a particular drain current falls within a specified range of values. It may also be required in some circuits to form both enhancement- and depletion-type units side-by-side on the same substrate. As shown by Eq. (1) these two types of units may have an identical set of characteristic curves differing only in the value of V_o, the gate voltage required for onset (or pinch-off) of drain current.

In the derivation of Eq. (1), the term V_o came from the density of surface states, n_o, initially present in the semiconductor through the relationship,

$$V_o = \frac{n_o L W q}{C_g} \tag{2}$$

where C_g is the total gate capacitance and dimensions L and W are defined in Fig. 3. Thus if n_o represents a large number of electrons initially present in an accumulation layer on the surface of the semiconductor, V_o is negative. On the other hand, if n_o represents a large number of unfilled acceptor states on the surface of the semiconductor, V_o is positive.

Figures 7 and 8 illustrate the way in which the energy bands at the surface of a semiconductor are bent by the presence of donor-like or acceptor-like surface states. For an enhancement-type TFT (V_o positive) it is necessary that the bands bend upward at zero gate bias forming an initial depletion layer at the semiconductor surface. Such an interface is usually obtained on the surface of a CdS layer which has been air-baked and then covered with a layer of calcium fluoride insulator. For a depletion-type TFT (V_o negative) the energy bands at the semiconductor surface bend down at zero gate bias

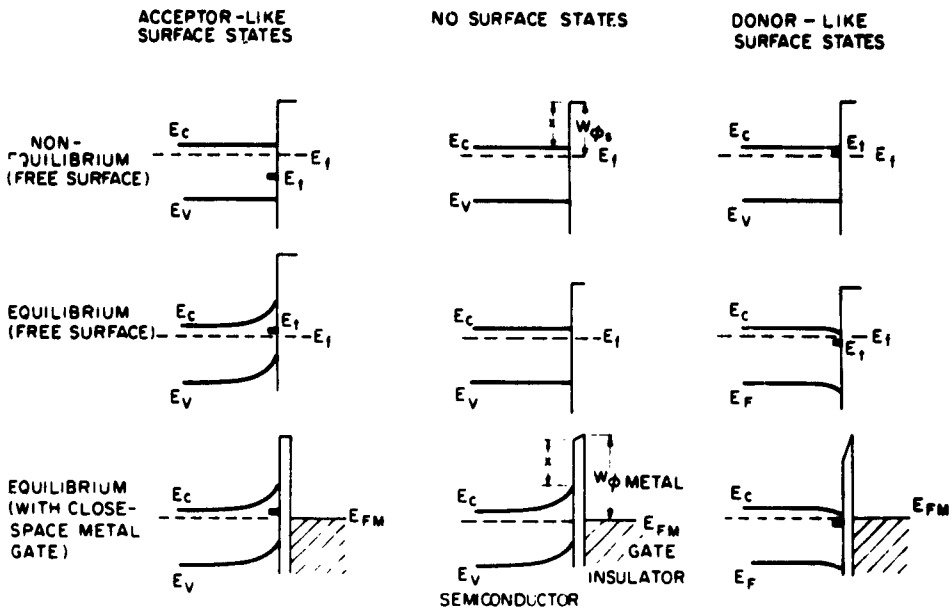


Fig. 7. The effect of surface states on the bending of the energy bands in the semiconductor at the gate interface.

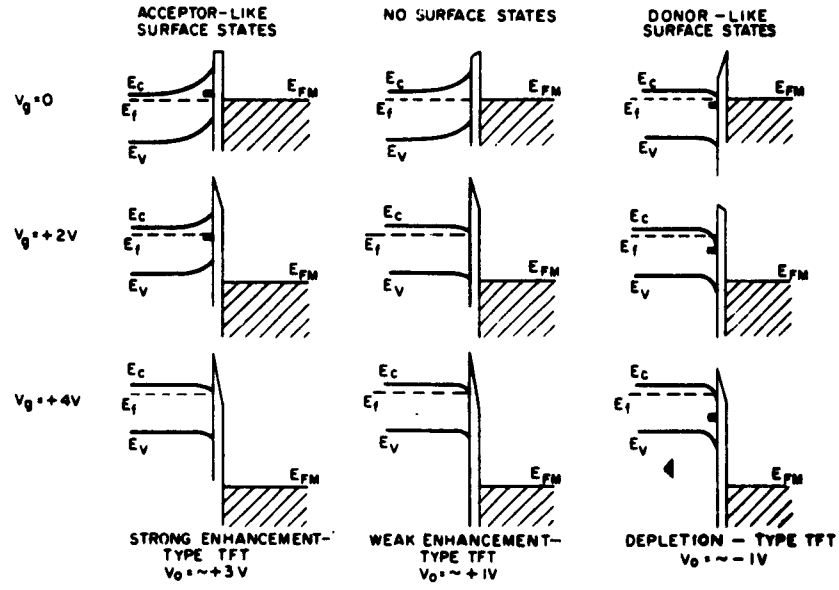


Fig. 8. The effect of surface states at the semiconductor-insulator interface upon the "built-in" gate bias V_o.

to form an accumulation layer. Such a contact can be formed on the surface of a cadmium sulfide layer by coating it with silicon monoxide evaporated under particular conditions. The control of V_o depends not only on the insulator but also upon the character of the cadmium sulfide surface.

It is apparent from the above discussion that the value of V_o can be controlled in the fabrication of the units by proper processing of the semiconductor layer and proper choice of the insulator. Other factors, such as the work function of the gate electrode, may also play a role. However, caution should be exercised in evaluating V_o in experimental units. If either slow surface states are present at the semiconductor-insulator interface or the dielectric relaxation time ($K\rho$) of the insulator layer varies throughout the thickness of the layer, a slow drift in V_o is observed. When such a condition prevails, a typical observation would be that as more positive gate-voltage steps are added on the curve tracer, all drain current curves slump down temporarily so that one observes an apparent increase in V_o. (The drain current at zero gate bias may slump from a milliampere to zero after application of a positive gate bias and require as much as a minute after removal of the positive bias to recover its initial value.) Such "rubbery" characteristics are believed to be more likely due to the internal charging of a nonhomogeneous insulator than to slow surface states, although the two effects are difficult to separate. Figure 9 shows how a graded resistivity in a nonhomogeneous insulator may give rise to either a temporary increase or decrease of V_o

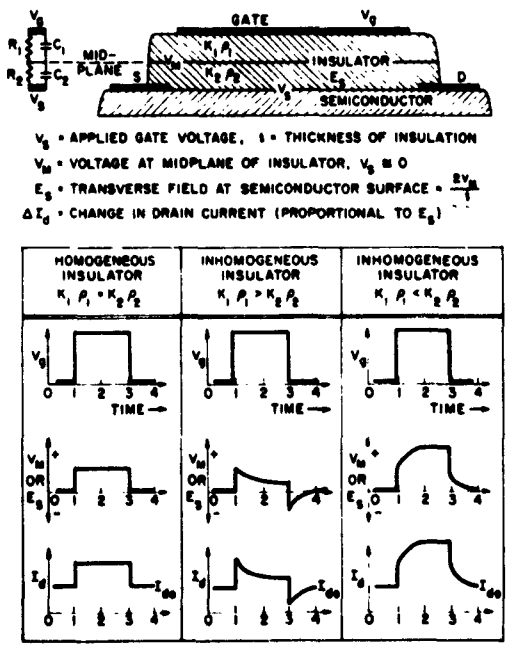


Fig. 9. The effect of a nonhomogeneous insulator having a graded dielectric relaxation time ($K\rho$) upon the slow speed response of an insulated-gate transistor. (A temporary suppression of I_{do} appears as a temporary increase in V_o.)

depending upon whether the resistivity of the insulator is higher or lower near the semiconductor interface. It is possible that in some fixed frequency applications not requiring D.C. operation, the nonhomogeneous insulator may provide a practical method of establishing an effective V_o.

For stable operation over a range of frequencies extending down to D.C., the above-mentioned "rubbery" characteristics are intolerable and present a fabrication problem for any insulated-gate transistor. Although such characteristics are frequently observed in the CdS TFT's, many units have been made which appear to be completely stable at D.C. and as displayed on the curve tracer. Work is continuing on obtaining a complete understanding and control of the stability problem.

2. Effect of Non-Ohmic Source-Drain Contacts

Normal operation of an insulated-gate field-effect transistor utilizing a high-resistance semiconductor requires a source contact having low impedance for injection of majority carriers. If the source contact impedance is not lower than the induced-channel impedance in the gap, a striking form of current saturation is introduced into the drain current-voltage characteristic. (See Fig. 10a)

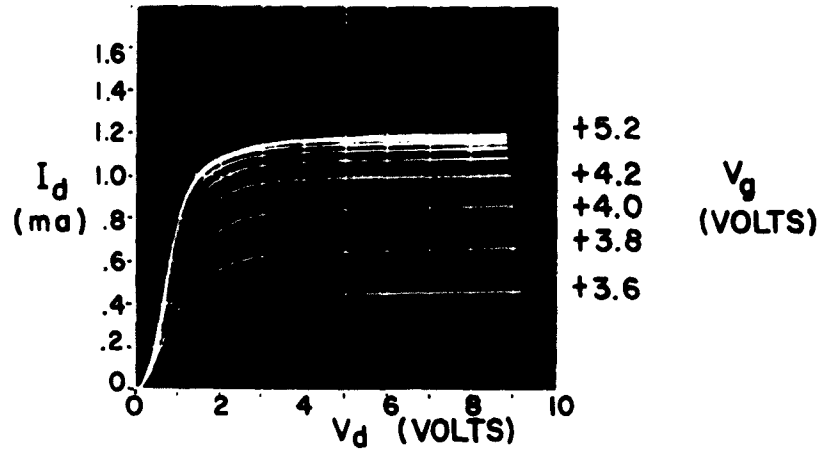


Fig. 10a. "Crowded" current-voltage characteristic observed in a TFT having an inadvertent insulating barrier under the source electrode.

Instead of continuing to increase with gate bias, the transconductance levels off and decreases toward zero as the family of curves crowd together at a maximum value of I_d. Although the "crowded" drain-current curves level off parallel to the normal saturated drain curves, the current-limiting action

of the source contact occurs quite independently of the control gate itself. Figure 10b shows a source-limited, saturated-current characteristic for a planar diode whose geometry is that of a TFT with the gate electrode omitted.

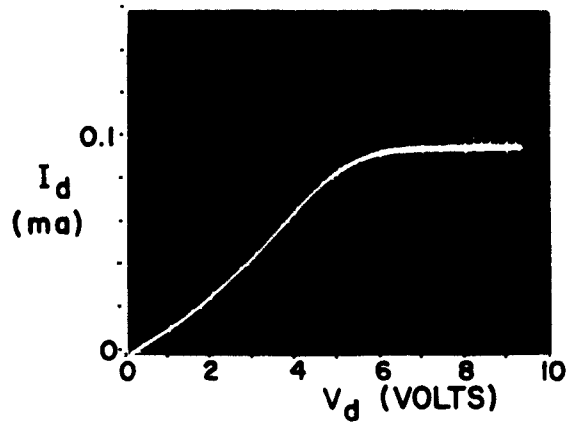


Fig. 10b. Saturated current-voltage characteristic having an insulating barrier under the cathode.

Inasmuch as other physical explanations can also be offered for the type of current-limiting action observed, the evidence for its being caused primarily by a barrier at the source will be reviewed. Since the presence or absence of "crowding" can be correlated with the technique of evaporation of the aluminum source electrode, it appears likely that the barrier, when present, consists of a layer of aluminum oxide under the source electrode too thick to be readily tunnelled by electrons. At low drain and gate voltages the normal accumulation-layer surface channel on the CdS extending back under the source electrode gives a large area of contact so that leakage through pinholes in the barrier is sufficient to supply the current required. (See Fig. 11a.) When the gate and drain voltage are increased the larger IR drop in the surface channel under the source electrode causes this channel to go positive with respect to the source thus pinching off the current at some maximum value. Since the current-limiting action under the source occurs by precisely the same pinch-off mechanism as that occurring under the gate giving rise to saturated drain characteristics in a normal TFT, it is no wonder that the two effects join together so smoothly in the characteristic of Fig. 10a. According to the above explanation an insulating barrier under the drain electrode would not lead to current saturation since the conductivity of the underlying channel would be strengthened

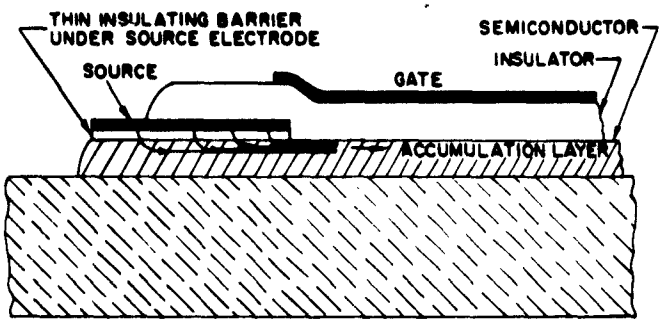


Fig. 11a. Current paths under the source electrode in a TFT having "crowded" characteristics. Electrons shown entering the accumulation layer on the semiconductor from the source via pin-holes in the barrier layer.

by the overlying positive drain. Thus if a TFT has an insulating barrier under only the source electrode it will yield normal "un-crowded" characteristics when the connections to the source and drain are reversed. The correctness of the above statements was demonstrated by the experimental TFT shown in Fig. 11b having a thin insulating barrier deposited under a portion of the drain electrode. When operated with the barrier at the drain the curves were normal, but when the electrode with the barrier was used as the source the characteristic curves were typically "crowded."

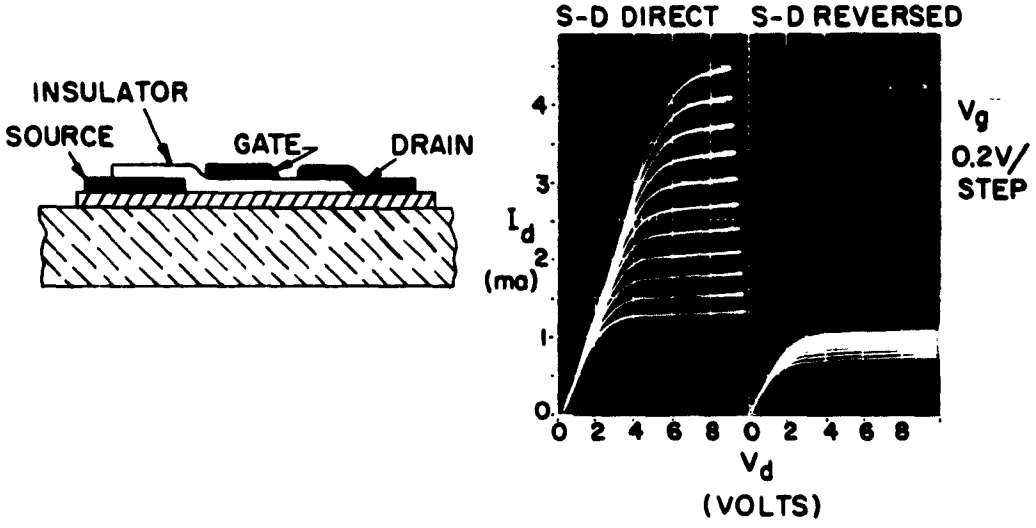


Fig. 11b. Demonstration of "crowded" characteristics of an experimental TFT having an insulated barrier deposited under a portion of one electrode. When operated with the barrier at the source the curves were typically crowded.

3. Factors Affecting the Life of the TFT

Although up until now the life characteristics of the TFT have not been thoroughly studied, the improved performance and increased opportunity for integrated-circuit applications will make this problem increasingly important. Most experimental CdS units which have not been encapsulated at all eventually degrade in characteristics regardless of whether they are operated or not. The rate of degradation for a 50% loss in g_m may vary from a period of a few hours to many months. (Fig. 12 shows a photo of the characteristics of the TFT used originally for Fig. 2b of Ref. 2 taken approximately four months later without encapsulation other than a plastic box containing some drying agent.)

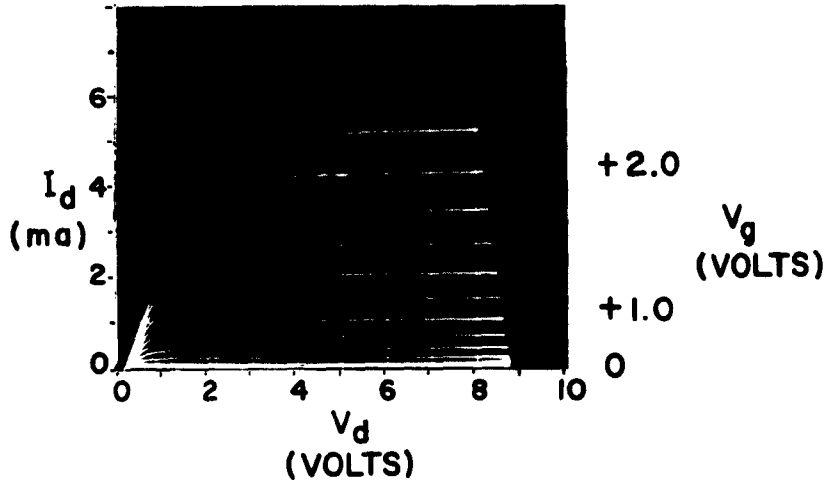


Fig. 12. Photograph of the characteristics of the CdS TFT used originally for Fig. 2b of Scientific Report No. 1 taken approximately four months later without encapsulation other than a plastic box containing a drying agent. The maximum transconductance has degraded about 20%.

Encapsulated units have not shown consistent improvement in life except for those units of a type which normally slump badly within a day or so on exposure to air. A part of the failure of encapsulation to provide indefinitely long life may be in the rather questionable methods of encapsulation which have been employed to date.

Many factors entering into the fabrication of the TFT which affect life need to be evaluated. The influence of humidity, oxygen, and other ambient conditions depends upon the fabrication procedures, which, in turn, must be chosen to meet the desired design characteristics. It is obvious

that from now on, stability and life problems must be approached from the same fundamental point of view as the investigation of the design and operating mechanisms of the TFT. The many-sided aspects of the life problem show up in the large variety of ways in which a unit may change in its characteristics sufficiently to be classed as a casualty.

E. THE CdSe COPLANAR TFT

Because of the separation of the semiconductor processing steps from the electroding steps in the coplanar TFT, this design is particularly well-suited to the study of other semiconductors for TFT applications. Work prior to the contract period had shown the feasibility of using cadmium selenide as the semiconductor in thin-film transistors.[5] These units had been made with both the normal and the inverted staggered electrode structure having the gate on the opposite side of the semiconductor from source and drain. They yielded transconductances above 10,000 micromhos together with voltage gains as high as 150. A number of problems were encountered with reproducibility of the units and with control of film resistivity. As the optimum deposition temperature for the CdSe appeared to be in the range of 250 to 300°C, electrodes underlying the CdSe had to withstand temperatures in this range without thermal damage. Use of the staggered structure made the units sensitive to series-resistance effects for high-resistivity films as well as requiring relatively good film homogeneity.

With the development of methods of fabricating high-performance CdS TFT's with a coplanar electrode structure, it became of interest to evaluate CdSe units made in a similar manner. The relatively high Hall mobilities in CdSe single crystals (about 500 cm^2/volt-sec) and the ease of deposition of CdSe films at relatively high substrate temperatures made this material attractive for TFT's. The high resistance obtained in many of the films suggested that units with low zero-bias current might be readily obtained in the coplanar structure. It was desirable to test the generality of fabrication techniques which had been successful for CdS units.

The cadmium selenide films were made by evaporation onto glass substrates in the 10^{-6} torr range. The evaporant was crystalline needles with total spectrographic impurities in the range of 10-50 ppm. Substrate temperatures were varied between 100 and 390°C. Film thickness was 600 to 4000 A. After deposition, some of the samples were given short bakes in air at about 500°C. Electrodes and insulator layers were then applied by vacuum evaporation with a procedure similar to that used with cadmium sulfide coplanar structures. Gap spacings were 0.4 mil and width of active area about 100 mils.

The performance of cadmium selenide units was sensitive to substrate temperature, processing, and electrode material. As in the case of cadmium sulfide, aluminum electrodes were considerably

superior to gold electrodes. Aluminum electrodes generally gave well-saturated characteristics and high g_m. There was no evidence of crowding on samples given the high-temperature bake when aluminum electrodes were used. However, a slight "S"-shape rise was observed for some low-substrate-temperature units having aluminum electrodes, which indicated some series diode effects. Units with gold contacts had low g_m, poor saturation, and some indication of crowding. Use of indium under the aluminum gave inconclusive results. A fairly large amount of indium (10% transmission to white light) caused a very high zero-bias drain current, apparently due to scattered indium in the source-drain gap. A smaller amount (80% transmission) gave results not significantly different from aluminum alone.

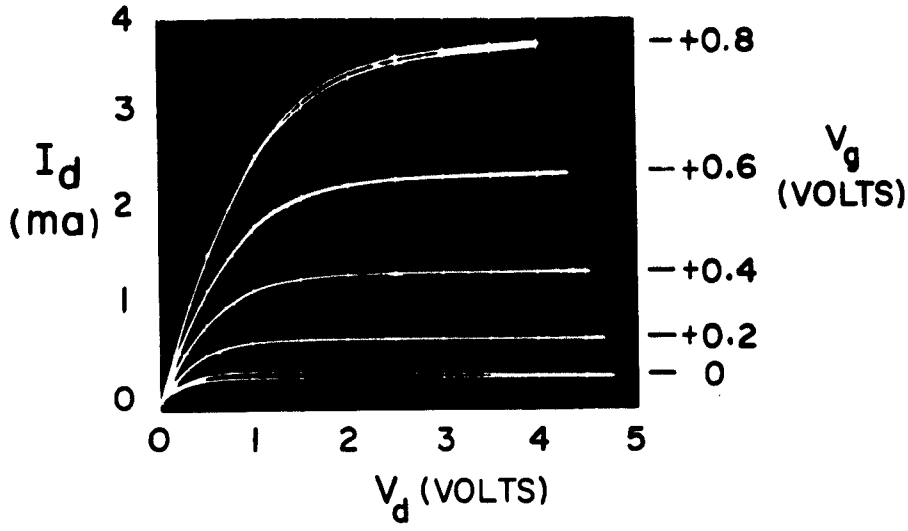
Increasing the substrate temperature for the CdSe deposition appeared to improve the performance, especially for samples which were not given high-temperature bakes. Units with CdSe deposited at high-substrate temperature were less subject to crowding, hysteresis loops, and "rubbery" characteristics (instability of operating characteristics with variations in bias) than were units deposited at low temperature. Use of the high-temperature bake tended to eliminate crowding effects and reduce the extent of hystersis loops.

The gate insulator used was SiO in amounts similar to that employed with CdS. Units with half the normal insulator thickness showed somewhat higher g_m, but were subject to relatively easy breakdown.

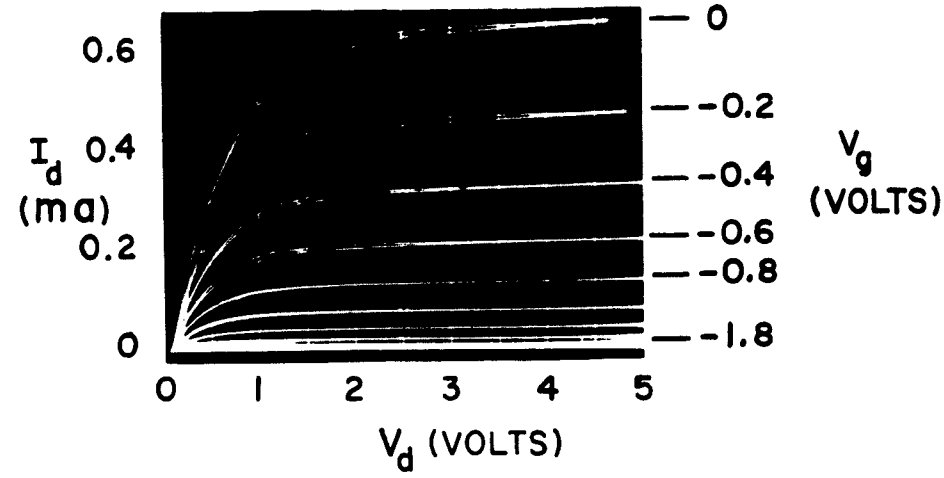
Changes in the units with time were similar to those observed with CdS. In general, the g_m at constant drain current was roughly constant for times of a least a week for unencapsulated units. However, the gate bias required for a given drain current increased with time. Use of a relatively heavy layer of SiO evaporated on top of the completed units caused a significant reduction in the rate of change in the gate bias needed for a given drain current.

Both enhancement and depletion operation was obtained. Some units showed zero-bias currents less than 1 μa, together with good saturation and transconductances of several thousand micromhos. Figure 13a shows the enhancement-mode characteristics of a unit with CdSe deposited on a 250°C substrate, with subsequent high-temperature air bake and aluminum electrodes. At V_d = 4 volts and V_g = 0.8 volt, the transconductance is 8000 micromhos, and the voltage gain is 100. In this unit source-drain current could be pinched off with a negative bias of 0.6 volts. Figure 13b shows the depletion-mode operation of a similar unit, having the CdSe deposited on a 390°C substrate.

The results obtained for CdSe coplanar units are qualitatively similar to those for CdS units made in a similar way, and are also comparable with those obtained for some staggered electrode



(a) ENHANCEMENT UNIT



(b) DEPLETION UNIT

Fig. 13. Drain characteristics of two coplanar CdSe TFT's.

units made with CdSe. As a relatively small amount of work has been devoted to the fabrication of CdSe coplanar structures, the results must be considered as preliminary and the fabrication parameters as not yet optimized.

F. THE FIELD-EFFECT DIODE

The excellent performance of the coplanar insulated-gate TFT has led to a proposal for a new type of diode which may be particularly useful in thin-film integrated-circuit applications. Although capable of high rectification ratios, the rectifying characteristics are based upon the field-effect action of a partially insulated electrode and not upon the use of dissimilar contacts. The principle of operation of the field-effect diode can be demonstrated by connecting the gate to the drain of an insulated-gate TFT as shown in Fig. 14. Three TFT's having different characteristics are considered; all have bidirectional characteristics with ohmic contacts at both source and drain, but with different values of built-in gate bias, V_o. When operated with the gate tied to the anode, the depletion-type unit in Fig. 14a has a rapidly rising characteristic in the forward direction, but a saturation characteristic in the reverse direction. The enhancement type in Fig. 14b, with $V_o = 0$ volts, has a forward characteristic which is concave upward starting at zero but has low conductance in the reverse direction. The strongly enhancement-type unit in Fig. 14c, having V_o positive, is also insulating in the reverse direction, but does not conduct in the forward direction until V_A is several volts positive.

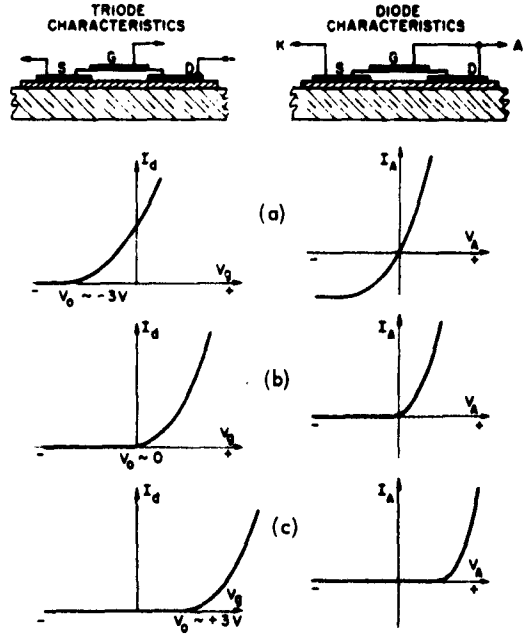


Fig. 14. Expected diode characteristics for an insulated-gate transistor having the gate tied to the drain for different values of V_o.

In practice, the field-effect diode can be made as shown in Fig. 15a, with both electrodes forming ohmic contacts to the semiconductor, or as in Fig. 15b, with one electrode blocking.

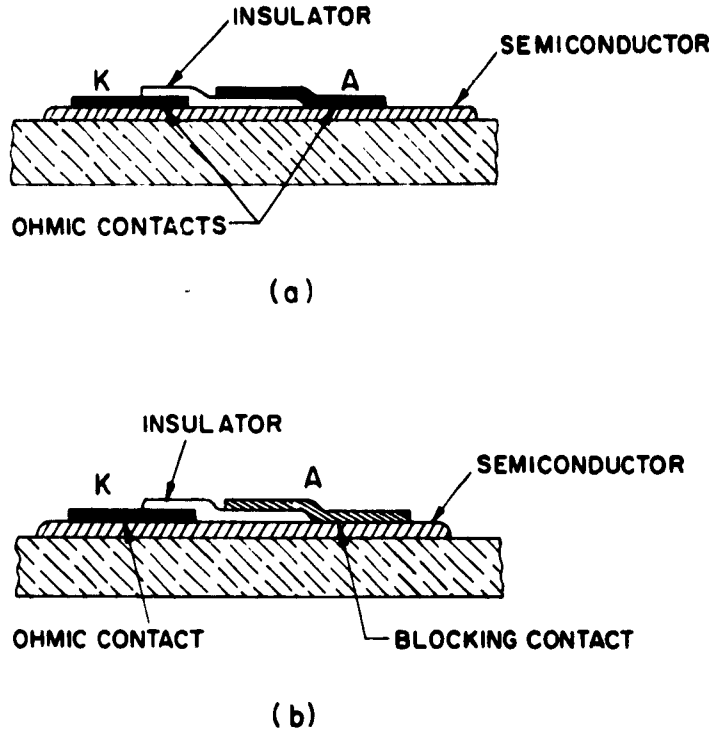


Fig. 15. Cross-sectional drawings of two forms of field-effect diodes.

Figure 16 shows some actual characteristics of TFT's having different values of V_o and connected as field-effect diodes. Rectification ratios up to 10^4 have been observed on units with ohmic contacts at both electrodes. With suitably high values of V_o the ratio should go considerably higher.

G. APPLICATION OF THE COPLANAR TFT TO INTEGRATED CIRCUITS

The new thin-film techniques which have been evolved in the development of the coplanar TFT show promise of greatly simplifying the fabrication of complex thin-film circuits. In addition to transistors and diodes, resistors can also be formed on the surface of the semiconductor by depositing material on top of the semiconductor which induces an accumulation layer. A thin overlayer of SiO can reduce the surface resistivity of a CdS layer by a factor of 10^4. Present indications

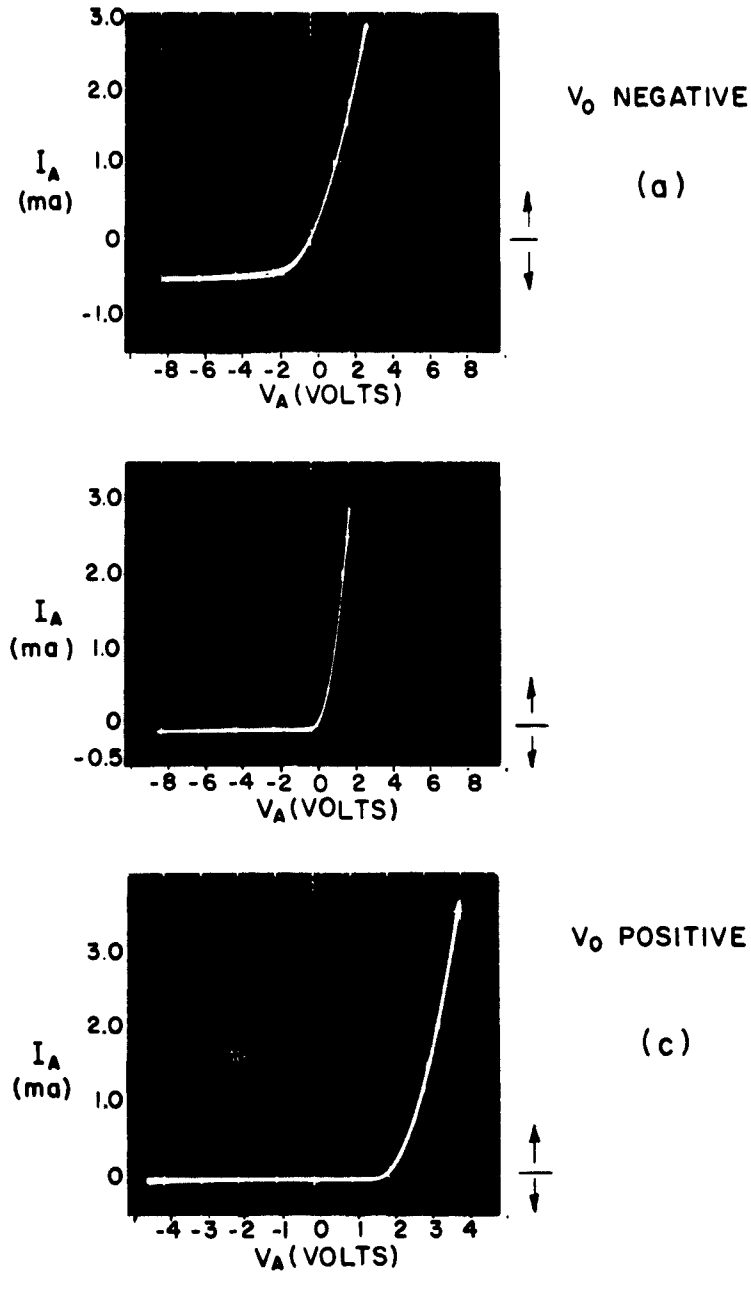


Fig. 16. Measured characteristics of three CdS TFT's having different values of V_o connected as field-effect diodes.

are that stable, linear resistors can be produced in this manner having a resistivity as high as 100,000 ohms per square. Such a high value permits the convenient fabrication of load resistors resistors for the TFT's in integrated circuits.

A project at RCA Laboratories (not supported by this contract) is directed toward the utilization of the TFT and related thin-film components in a particular device application. In this application still another characteristic of the cadmium sulfide will be utilized: its photoconductivity. In such applications the ability to deposit the entire structure upon a transparent insulating substrate permits structures not possible following conventional single-crystal-silicon integrated-circuit methods. The coplanar TFT with related diodes and resistors offers a powerful new approach to integrated circuits of a most complex character.

III. THIN-FILM MATERIAL STUDIES

A. MOBILITY MEASUREMENTS

A further examination was made of Hall mobility vs. temperature data taken on operating TFT's. In Fig. 17 a plot is given of log μ_H, log I_d and log (I_d/μ_H) vs. 1/T, where μ_H is the measured Hall mobility and I_d the drain current. The data were taken with 2 volts gate bias. Both I_d and μ_H show on exponential dependence on 1/T. Petritz[6] has shown that the presence of intercrystalline barriers

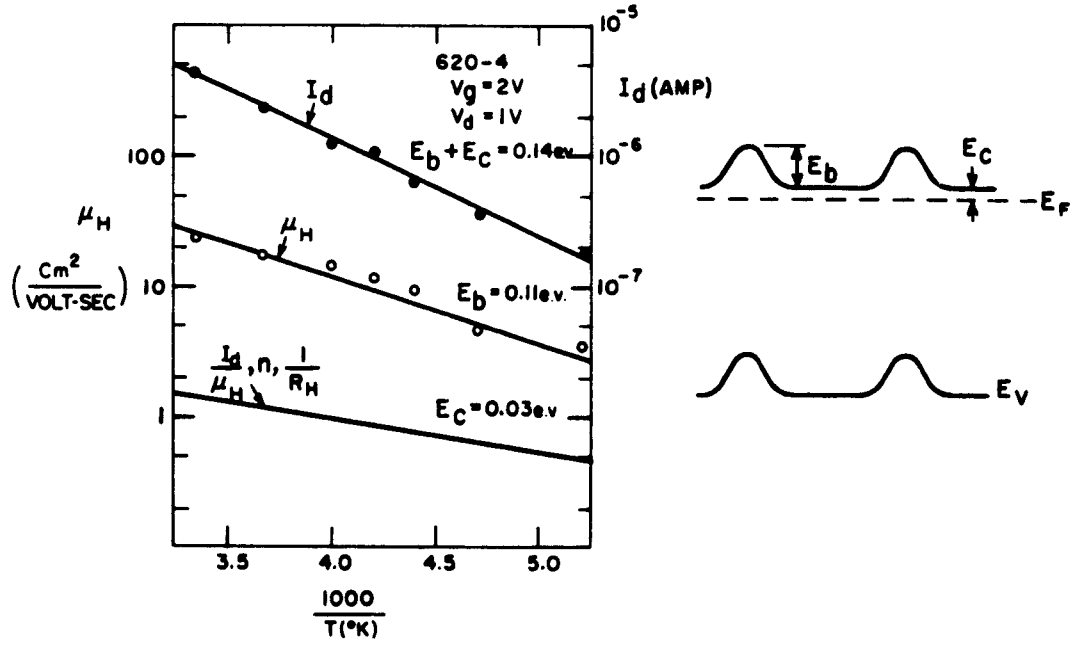


Fig. 17. Temperature dependence of Hall mobility and conductance in a TFT Hall sample and band structure for a possible barrier model.

in a film should give an effective Hall mobility having an exponential dependence on 1/T, with an activation energy equal to the barrier height. Assuming a similar model for CdS,[2] the drain current divided by the measured Hall mobility is proportional to the number of carriers and to the Hall coefficient. I_d/μ_H will yield an activation energy which is a measure of the depth of the Fermi level from the conduction band, and depends on the position of trapping levels in the semiconductor. The drain current should have an activation energy equal to the sum of the two

previous activation energies. The indicated barrier height is thus about 0.14 ev. It is expected that additional mobility data will be obtained to permit more detailed analysis of the possible barrier structure in these films.

Mobility measurements on larger area samples, without gates, have been made using 6-electrode methods to evaluate variations in CdS processing and to obtain additional information about the film structures. It was found that as deposited, the CdS films had measured Hall mobilities of 0.3 to 2.3 cm^2/volt-sec in the dark. Samples given high-temperature air bakes showed measured dark mobilities in the range of 3.6 to 91 cm^2/volt-sec. Samples with the lowest dark mobilities had aged at room temperature for several weeks; they showed the largest increase in mobility under illumination, suggesting a possible change in barriers with time. The mobilities under illumination (about 1 watt/cm^2) varied between 2.4 and 3.6 cm^2/volt-sec for unbaked samples and 35 to 110 cm^2/volt-sec for baked samples. The mobility did not appear to be very dependent on deposition rate. Use of a heavy SiO layer over the sample appeared to produce an increase in mobility as well as a decrease in sample resistance, consistent with the formation of an accumulation layer in the CdS analogous to that produced by field effect in the TFT.

B. MATERIALS AND TECHNIQUES

During this period a more detailed examination of cadmium sulfide evaporation parameters was carried out. The relation between evaporation temperature and deposition rate was studied as were the effects of modification in evaporator design. For our usual spherical alundum-coated evaporator, the evaporator temperature, as measured by both thermocouple and optical pyrometer, is about 1000°C for a deposition rate of 90 A/sec and a 180°C substrate temperature. The rate appears to rise less rapidly with evaporator temperature than expected from vapor pressure data. This probably indicates a nonequilibrium situation in the evaporator.

A relatively large area, low-temperature evaporator, in which the cadmium sulfide was placed in a quartz holder and heated by radiation, gave deposition rates of the order of 45 A/sec for a source temperature of 820°C. Use of this type of evaporator permitted evaporation at temperatures of about 700°C. The sample resistivity appeared to increase with evaporator temperature, in contradiction to the results expected if the extent of CdS dissociation were increasing substantially with temperature in the evaporation range. The TFT's made in this manner did not appear significantly different from those made by the normal method.

Cadmium sulfide films prepared in another RCA group by vapor transport methods are being evaluated for their suitability for use in TFT's. Several films in a usable resistance range have

been examined. Our present fabrication techniques appear suitable for use with these films, although at present there is a problem in making a sufficiently low-resistance contact. One set of these units has shown some enhancement-type TFT operation.

Several metal oxides were prepared by reactive sputtering for evaluation in TFT structures. Zinc oxide, a II-VI semiconductor like CdS and CdSe, was successfully fabricated into coplanar-type TFT's. The ZnO units showed transconductances of several hundred micromhos, and some saturation. Cadmium oxide was prepared by this method to investigate its possible role in standard TFT's; the films were highly resistive and did not show TFT action. Preliminary work on sputtered copper and nickel oxides was also done. Work was continued on evaluation of the III-V compounds indium antimonide and gallium arsenide.

IV. GENERAL FACTUAL DATA

A. PERSONNEL

Individuals who contributed to the contract activity during this report period were:

H. Borkan
F. V. Shallcross
P. K. Weimer

Fabrication and testing of experimental units were carried cut by V. L. Frantz, W. S. Homa, H. P. Lambert, and R. G. Pugliesi.

B. VISITORS, CONFERENCES AND TRAVEL

Conferences

P. K. Weimer attended the Solid-State Circuits Conference at the University of Pennsylvania, University of Pennsylvania, Philadelphia, Pa., on February 17, 1963.

Travel

P. K. Weimer visited the Wright-Patterson Air Force Base at Dayton, Ohio, on January 30, 1963.

C. PUBLICATIONS

F. V. Shallcross, "Cadmium Selenide Thin-Film Transistors" *Proc. IEEE*, in press, covering work done prior to the contract.

H. Borkan and P. K. Weimer, "An Analysis of the Characteristics of Insulated-Gate Thin-Film Transistors," *RCA Review*, in press.

P. K. Weimer, "Physical Processes in the Insulated-Gate Thin-Film Transistor" – talk given at the Xerox Corporation, Rochester, New York, on January 16, 1963.

REFERENCES

1. P. K. Weimer, "The TFT – A New Thin-Film Transistor," *Proc. IRE*, Vol. 50, pp. 1462-1469, June 1962.

   P. K. Weimer, "An Evaporated Thin-Film Triode" presented at the IRE-AIEE Device Research Conference, Stanford University, California, June 1961.

2. P. K. Weimer, H. Borkan, V. E. Henrich, and F. V. Shallcross, "Evaporated Thin-Film Devices – Scientific Report No. 1" AFCRL-62-965, Nov. 1962.

3. H. Borkan and P. K. Weimer, "Characteristics of the Insulated-Gate Thin-Film Transistor," IRE, *NEREM Record*, pp. 158-159, Nov. 1962.

4. H. Borkan and P. K. Weimer, "An Analysis of the Characteristics of Insulated-Gate Thin-Film Transistors," *RCA Review*, in press.

5. F. V. Shallcross, "Cadmium Selenide Thin-Film Transistors," *Proc. IEEE*, in press.

6. R. L. Petritz, et al., "Surface Studies on Photoconductive Lead Sulfide Films," *Semiconductor Surface Physics*, University of Pennsylvania Press, Philadelphia, Pa., p. 229, 1957.

Air Force Cambridge Research Laboratories, Bedford, Massachusetts. Rpt. No. AFCRL-63-67. EVAPORATED THIN-FILM DEVICES. Scientific Report No. 2, March, 1963, 33 p. incl illus., tables and 6 ref.

Unclassified Report

An improved electrode arrangement for the insulated-gate thin-film transistor has yielded higher performance and greater ease of fabrication. "On-to-off" current ratios of 10^7, input resistance exceeding 10^{10} ohms, & gain-bandwidth products of 25 megacycles have been obtained with polycrystalline cadmium sulfide films. By depositing all electrodes on top of the semiconductor, maximum freedom in processing the semiconductor layer is obtained. A novel type of field-effect diode is described.

1. Transistors
2. Semiconducting films
3. Semiconductors
4. Cadmium sulfide films

I. Project 4608, Task 460804
II. Contract AF19(628)-1617
III. Radio Corporation of America, Princeton, New Jersey
IV. P.K. Weimer, H. Borkan, F.V. Shallcross
V. In ASTIA collection

Air Force Cambridge Research Laboratories, Bedford, Massachusetts. Rpt. No. AFCRL-63-67. EVAPORATED THIN-FILM DEVICES. Scientific Report No. 2, March, 1963, 33 p. incl illus., tables and 6 ref.

Unclassified Report

An improved electrode arrangement for the insulated-gate thin-film transistor has yielded higher performance and greater ease of fabrication. "On-to-off" current ratios of 10^7, input resistance exceeding 10^{10} ohms, & gain-bandwidth products of 25 megacycles have been obtained with polycrystalline cadmium sulfide films. By depositing all electrodes on top of the semiconductor, maximum freedom in processing the semiconductor layer is obtained. A novel type of field-effect diode is described.

1. Transistors
2. Semiconducting films
3. Semiconductors
4. Cadmium sulfide films

I. Project 4608, Task 460804
II. Contract AF19(628)-1617
III. Radio Corporation of America, Princeton, New Jersey
IV. P.K. Weimer, H. Borkan, F.V. Shallcross
V. In ASTIA collection

Air Force Cambridge Research Laboratories, Bedford, Massachusetts. Rpt. No. AFCRL-63-67. EVAPORATED THIN-FILM DEVICES. Scientific Report No. 2, March, 1963, 33 p. incl illus., tables and 6 ref.

Unclassified Report

An improved electrode arrangement for the insulated-gate thin-film transistor has yielded higher performance and greater ease of fabrication. "On-to-off" current ratios of 10^7, input resistance exceeding 10^{10} ohms, & gain-bandwidth products of 25 megacycles have been obtained with polycrystalline cadmium sulfide films. By depositing all electrodes on top of the semiconductor, maximum freedom in processing the semiconductor layer is obtained. A novel type of field-effect diode is described.

1. Transistors
2. Semiconducting films
3. Semiconductors
4. Cadmium sulfide films

I. Project 4608, Task 460804
II. Contract AF19(628)-1617
III. Radio Corporation of America, Princeton, New Jersey
IV. P.K. Weimer, H. Borkan, F.V. Shallcross
V. In ASTIA collection

Air Force Cambridge Research Laboratories, Bedford, Massachusetts. Rpt. No. AFCRL-63-67. EVAPORATED THIN-FILM DEVICES. Scientific Report No. 2, March, 1963, 33 p. incl illus., tables and 6 ref.

Unclassified Report

An improved electrode arrangement for the insulated-gate thin-film transistor has yielded higher performance and greater ease of fabrication. "On-to-off" current ratios of 10^7, input resistance exceeding 10^{10} ohms, & gain-bandwidth products of 25 megacycles have been obtained with polycrystalline cadmium sulfide films. By depositing all electrodes on top of the semiconductor, maximum freedom in processing the semiconductor layer is obtained. A novel type of field-effect diode is described.

1. Transistors
2. Semiconducting films
3. Semiconductors
4. Cadmium sulfide films

I. Project 4608, Task 460804
II. Contract AF19(628)-1617
III. Radio Corporation of America, Princeton, New Jersey
IV. P.K. Weimer, H. Borkan, F.V. Shallcross
V. In ASTIA collection